Attorney's Docket No.: 10559-403001 / P10340

REMARKS

Reconsideration and allowance of the above-referenced application are respectfully requested.

Upon entry of this amendment, claims 1-17 will remain in the application.

Claims 1 and 2 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada et al. (US 6,225,846), hereinafter Wada, in view of Fujita et al. (US 6,215,159), hereinafter Fujita.

Claims 3-17 were rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Wada in view of Fujita and further in view of Rossi et al. (US 6,069,513), hereinafter Rossi.

Applicants respectfully traverse these rejections.

Applicants teach a dynamic bus repeater circuit with an improved noise margin of Vcc/2. This noise margin is closer to that of a static bus repeater than standard dynamic repeaters which may have a noise margin only slightly higher than the threshold voltage of the input transistor. The bus repeater is a dynamic circuit, i.e., it is clocked and has a pre-charge stage in which the value on the input node does not affect the output, and an evaluation stage in which the value on the input does affect the output.

Wada discloses static voltage divider circuit (4), which contains no clocked inputs. Rather than improving the noise margin of a dynamic bus repeater circuit, the voltage divider is provided to reduce the threshold voltages of the inverters (1) and (2) to improve switching speed (col. 4, ll. 60-64).

The present Action and the previous Action mailed April 10, 2002 fail to address the limitation in independent claim 1 of "an output node operative to output a voltage of Vcc/2 in

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response to a voltage of Vcc/2 on the input node in the evaluate mode" and the limitation in independent claim 11 of "a dynamic repeater... having a noise margin of Vcc/2." None of Wada, Fujita, and Rossi teach or suggest a dynamic repeater having a noise margin of Vcc/2. Accordingly, the Action has failed to make a prima facie showing of obviousness.

Furthermore, Wada makes no provisions for maintaining, let alone improving, the noise margin in the modified circuit. Applicants submit that Wada teaches sacrificing the noise margin in the circuit for reduced threshold voltage and switching speed. Accordingly, Wada teaches away from improving the noise margin of the circuit.

Applicant asks that all claims be allowed.

Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 3 DEC 2002

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